CLAIMS:

1. A method for simulating operation of at least a portion of an integrated circuit for determining dynamic power dissipation associated therewith, comprising:

dividing the integrated circuit into at least one cell;

identifying at least one node associated with the at least one cell;

providing parameters, other than frequency, for determining dynamic power dissipation of the at least one node;

simulating operation of the at least one cell;

counting transitions of the at least one node to provide an activity factor;

dividing the activity factor by simulation time to obtain the frequency; and

calculating dynamic power dissipation for the at least one node.

2. The method of claim 1 wherein the at least one node is a clock node.

3. The method of claim 1 wherein the at least one node is a data node.

4. The method of claim 1 wherein the at least one node is a combinatorial logic node.

5. The method of claim 1 wherein the at least one node is a sequential circuitry node.

6. The method of claim 5 wherein the sequential circuitry node is a toggle flip-flop node.

7. The method of claim 1 wherein the integrated circuit is selected from a field programmable gate array (FPGA), an application specific integrated circuit (ASIC) and a complex programmable logic device (CPLD).

8. The method of claim 1 wherein the at least one cell is a macrocell.

9. The method of claim 1 wherein the dynamic power dissipated is calculated by multiplying a capacitive load associated with the at least one node by source voltage squared and by the frequency.

10. A method for determining dynamic power dissipation, comprising:

providing a general-purpose computer programmed with a simulator;

providing a model of an integrated circuit to the general-purpose computer;

providing signal generating code to the simulator;

providing power characteristic data, other than an activity factor, to the general-purpose computer;

generating power dissipation code using at least a portion of the model and the power characteristic data;

annotating the model using the power dissipation code to provide an annotated model;

providing the annotated model to the simulator;

simulating operation of the integrated circuit with the simulator in response to the annotated model and to the signal generating code; and

determining dynamic power dissipated by the integrated circuit under simulated operation using the annotated model.

11. The method of claim 10 wherein the model is a Very High Level Description Language (VHDL) model of the integrated circuit.

12. The method of claim 10 wherein the power dissipation code comprises determining the activity factor associated with a circuit element of the integrated circuit.

13. The method of claim 12 wherein the activity factor is divided by simulation time to provide frequency of operation of the circuit element.

14. A signal-bearing medium containing a simulation program which, when executed by a processor in response to receiving an integrated circuit model and power characteristic data, causes execution of a method comprising:

generation of power dissipation code; and

annotation with the power dissipation code of a testbench configured for the integrated circuit model.

15. A signal-bearing medium containing a simulation program which, when executed by a processor in response to receiving a integrated circuit model and power characteristic data, causes execution of a method comprising:

generation of power dissipation code; and

annotation with the power dissipation code of the integrated circuit model.

16. A method of determining dynamic power dissipation for a model of an integrated circuit, comprising:

dividing at least a portion of the integrated circuit into a plurality of cells;

identifying nodes within each of the cells;

ascribing a capacitive load value to each node of the nodes;

declaring states for each of the nodes;

simulating operation of the integrated circuit;

counting transitions for each of the nodes when going from one of the states to another of the states; and

determining dynamic power dissipated at each of the nodes.

17. The method of claim 15 wherein the step of determining dynamic power dissipated comprises:

dividing a count from the step of counting transitions by a simulation time for each of the nodes to provide a switching frequency for each of the nodes; and

multiplying the switching frequency for each of the nodes by square of a source voltage and by the capacitive load value of the node for each of the nodes.

18. The method of claim 17 further comprising summing the dynamic power dissipated for each of the nodes.

19. The method of claim 18 further comprising:

multiplying standby current by the source voltage to provide a product; and

adding a sum from the step of summing to the product.

20. The method of claim 17 wherein the dynamic power dissipated is determined prior to ending a simulation of the integrated circuit.

21. A method for determining dynamic power dissipation, comprising:

providing a general-purpose computer programmed with a simulator;

providing a model of an integrated circuit to the simulator;

providing signal generating code;

providing power characteristic data, other than an activity factor, to the general-purpose computer;

generating power dissipation code using a portion of the model and the power characteristic data;

annotating the signal generating code using the power dissipation code to provide annotated signal generating code;

providing the annotated signal generating code to the simulator;

simulating operation of the integrated circuit with the simulator in response to the model and to the annotated signal generating code; and

determining dynamic power dissipated by the integrated circuit under simulated operation using the annotated signal generating code.

22. The method of claim 21 wherein the model is a Verilog model of the integrated circuit.

23. The method of claim 21 wherein the power dissipation code comprises determining the activity factor associated with a circuit element of the integrated circuit.

24. The method of claim 23 wherein the activity factor is divided by simulation time to provide frequency of operation of the circuit element.